

Hybrid Domino XOR Gate with Dual Threshold Voltage Transistors

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Abstract

At the present time, in integrated circuit technology CMOS, low power design is an important subject in system design. In order to achieve this target, power consumption must be minimized. In this article two new domino XOR gates in 45nm technology are presented. First proposed circuits adopt hybrid transistor topology in the pull-down network with all transistors being low threshold voltages. A second proposed circuit adopts hybrid topology with dual threshold voltage transistors. By eliminating two input inverter and preventing the pulse flow to the output node during the precharge phase, power consumption in this circuit is reduced. First proposed circuit reduces active mode power consumption by 78.91% and 54.55% as compared to standard N-type domino XOR and P-type domino XOR.. Similarly, second proposed circuit reduces active mode power consumption by 81.43% and 59.98% as compared to standard N-type domino XOR and P-type domino XOR.

Keywords: low power ; domino XOR gate; evaluation phase; precharge phase.

1. Introduction

Low power has become main constrain for portable systems. These systems require more feature and high battery life time. The total power of the electronic circuit is the sum of static power, dynamic power and short circuit power [1]. In nanometer regimes, dynamic power consumption becomes significant contributor to over all power consumption [2,3]. Hence, the reduction of power consumption is compulsory. After studying various techniques in literature found that domino circuits require less power consumption than static circuits [4-6]. The operation of domino circuits is based on charging and discharging of output node capacitance.

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These circuits are applied for higher speed of the system [7]. The XOR is one of the most critical components of a processor, as it is used in the automatic logic unit (ALU). Domino logic circuits are used in applications such as memory [8] microprocessor and digital logics [9] etc.

CMOS XOR has complex pull up and pull down networks, which results in high power consumption, large layout area, and low speed. Domino XOR has small layout area, low power consumption, and improved speed as compared to CMOS XOR [10].

Due to its superior performance and low power consumption, domino XOR is being used in many VLSI applications. Standard domino XOR gate requires two phase input signals, one is the original and the other is inverted signal. It needs additional inverters to meet the design requirements. The additional inverters not only increase the power consumption but also affect the performance of the circuit.

Power dissipation of the domino circuit is divided into three components [12]:

$$P_{\text{Total}} = P_{\text{Dynamic}} + P_{\text{Leakage}} + P_{\text{Short Circuit}} \quad (1)$$

P_{Total} : is Power dissipation of the device.

P_{Dynamic} : is the power consumed during capacitance charging and discharging.

P_{Leakage} : is the total leakage power of the circuit and this power increases as the technology is scaled down.

$P_{\text{Short Circuit}}$: is the power dissipated when direct current flows from power supply to ground.

1.1. Dynamic Power Consumption

Dynamic power consumption is observed when the circuit is in its active mode. It means that this power is consumed in the process of transition, processing procedure or data transferring.

This part of the power can be modeled as a result of charging and discharging of capacitive nodes in consecutive cycles. Hence in one cycle the capacitors through a series of paths are charged and in the next cycle through other routes in ground orbit are discharged.

The dynamic power consumption is calculated from the following equation:

$$P_{\text{Dynamic}} = \sum_i a_i V_{\text{DD}}^2 C_i \quad (2)$$

a_i : activity switching of the i th circuit node and a statistical parameter.

V_{DD} : power supply voltage, and C_i : the seen capacitor in the i th circuit node.

In order to decrease this power in accordance with the formula, it is enough to reduce the amount of one or more

of the parameters specified in the linkage. Except a_i statistical parameter which is determined based on circuit activity and the number of switches in a period of the clock signal frequency, two other factors with the advancement of semiconductor technology components have been reduced. So that by shrinking the transistor channel length, the circuit node of the capacitor that depends on the length and width of the channel is reduced. In addition, due to the smaller size of transistors and failure issues in transistor links, the supply voltage should also reduce accordingly.

In this case, improvements in operation technology and smaller size of transistors also lead to increased speed and reduced power consumption caused by the switching. In fact, the scaling method of transistors in this case are significant. In these methods various techniques are used in sizing transistors to achieve the optimal capacitor C_i in one side and optimized transistors currents on the other side to reach the lowest dynamic power consumption and highest speed digital integrated circuits.

1.2. Short Circuit Power Consumption

By considering the fact that MOSFET transistors do not work like ideal keys while shifting from connected mode to the disconnected mode and vice versa, they are in a state of semi-connected mode in which the lost power in transition process is called power consumption caused by short circuit.

For example, in an inverter circuit, once a transistor must be entirely disconnected and another transistor must be entirely connected: both transistors are turned on in which one transistor is connected to the power supply and the other one is connected to the ground circuit which causes power loss at a given instant.

Mathematical equation is as follows:

$$P_{\text{Short Circuit}} = a_i I_{\text{SC}} V_{\text{DD}} \quad (3)$$

I_{SC} for domino logic gate is the contention current that flows between the evaluation network and pMOS keeper during evaluation mode. This power dissipation must be kept low for better operation of the domino circuit.

1.3. Leakage Power Consumption

Leakage Power Consumption is equal to multiplication of leakage current in power supply circuit voltage:

$$P_{\text{Leakage}} = I_{\text{Leakage}} V_{\text{DD}} \quad (4)$$

Where I_{Leakage} is the combination of subthreshold and gate oxide leakage current.

In this article, we have used a combination of N-type and P-type transistors in the Pull Down network and have suggested switching-aware techniques to minimize the additional switching in which all transistors have low threshold voltage.

Then, the following topics will be discussed as follows:

In Section 2 describes the operation of the standard domino XOR circuit. In section 3, proposed circuits are discussed in details. In section 4, simulation & analysis are presented and in section 5 we will draw a conclusion.

2. Standard domino xor gate

Domino logic is basically a dynamic logic circuit followed by a static inverter and having a capacitor as a load. The clock signal is used to control the operation of domino logic circuit [13]. The output of the dynamic logic circuit is stored in the parasitic capacitance which is located just before the static inverter [14]. The standard N-type domino XOR gate (DXN) is shown in Figure.1. M2 act as charge keeper. Pull down network consists of combination of n-type transistors. Here dynamic node gives XNOR gate logic $V_n = A \odot B$ and the output node gives XOR gate logic $V_{Out} = A \oplus B$. Operation of the circuit (precharge and evaluation phase) depends on the state of clock signal. When clock is low, the circuit is in precharge phase. Dynamic node is charged to high voltage by the pull up transistor M1. Footer transistor M5 turns OFF to avoid short circuit current in the circuit. When clock is high, the circuit is in evaluation phase. M1 turns OFF and M5 turns ON. Discharging of dynamic node is decided by the combination of inputs of the circuit. If $A=0, B=1$ or $A=1, B=0$, dynamic node turns to low voltage and output node turns to high voltage. Output node remains low for the other input states .

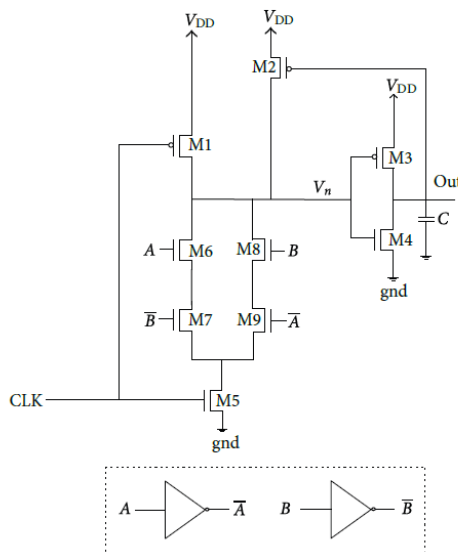


Figure 1: Standard N-type domino XOR gate (DXN). [15]

The standard p-type domino XOR gate (DXP) as shown in Figure.2[16].

M2 act as charge keeper. Pull up network consists of combination of p-type transistors. Working of the circuit is explained as follows: During precharge phase, charging of dynamic node depends on the combination of inputs. If $A=0, B=0$ or $A=1, B=1$, dynamic node is charged to high voltage and output node is discharged to low

voltage.

For other inputs state, output remains high. During evaluation phase dynamic node is discharged to low voltage and output node is charged to high voltage.

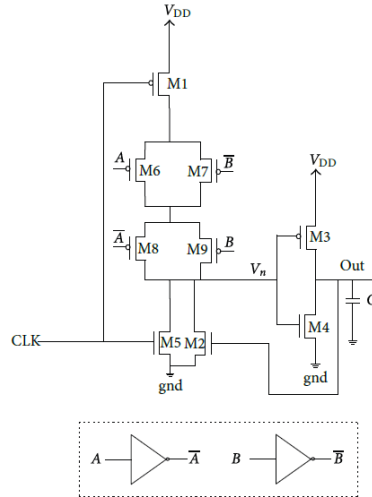


Figure 2: Standard P-type domino XOR gate (DXP). [15]

P-type domino XOR gate has a great advantage as compared to N-type domino XOR. It effectively suppresses both subthreshold and gate oxide leakage current at the expense of speed. N-type domino circuit has higher speed and higher power consumption, and P-type domino circuit has lower speed and lower power consumption. Drawbacks of standard N-type or P-type is that the input signals must have two phases, original and its inverted signals. Extra inverters must be added in the circuit to get inverted signal of original signal. Adding inverter increases the extra power consumption and propagation delay which extremely affects the performance of the domino XOR gate.

3. Proposed domino xor gate structures

N-type transistors have high speed and P-type transistors have low power consumption. In the following suggested circuits, we will use the advantages of these two type transistors N and P together. Propagation of precharge pulse during precharge phase in standard domino logic circuit increases the switching activity at the dynamic node and output node. This increases the power consumption and output node is unstable. This problem is overcomes by proposed circuit1 and proposed circuit2. Proposed circuits minimize redundant switching at output node.

3.1. Proposed Circuit 1

This technique uses the combination of N-type and P-type transistor switches in the Pull Down network and using the dynamic node when the circuit is in precharge phase, the output circuit does not change as shown in Figure 3, Here all transistors low threshold voltage transistors. The drain of M2 is connected to the dynamic

node and its source is connected to the gate of transistor M4. The gate of M2 is connected to M through inverter. The source of the M4 transistor is also connected to the M5 transistor. Using this technique, it avoid precharge pulse not to propagates to the output node. Operation of this circuit is explained by considering the input logic. When both input signals are low i.e. A=B=0 or A=B=1, dynamic node remains high regardless of operating phase and output node is kept low. When both input signals are at different logic state, i.e. A=0 and B=1 or A=1 and B=0, there are two different cases depending on the operating phase.

1) During evaluation phase, M5 turns on and M1 turns off, dynamic node and M node is discharge to ground. Transistor M3 turns on and charges the output node to VDD. M2 turns on due to low voltage at M node. M2 pass low dynamic voltage to the gate of M4, this turns off the M4.

2) During precharge phase, transistor M5 is off, pull up transistor M1 precharge the dynamic node and M node is charge to high voltage due to parasitic capacitance at this node. High voltage at M mode turns off the transistor M2, which turns off the M4 and it helps the output node to hold its previous value. In this circuit topology, output node is isolated from ground during precharge phase means it helps to avoid propagation of precharge pulse to the output node.

In the above offered circuit, there is no need to reverse the input signals. As a result, it occupies less layout area compared to the standard domino XOR gate N-type and P-type. In this circuit, the inverter and transistor M2 in the pre-charge phase disconnect the output from the circuit. This will cause the pre-charge phase if the input value is changed, the output does not change any more to avoid power wasting. Since additional inverters have been removed the input power is reduced too. Dynamic node gives XNOR and output node offers XOR logic.

$$V_n = \overline{(\overline{A} + \overline{B}) \cdot (A + B)} \Rightarrow V_n = A \cdot B + \overline{A} \cdot \overline{B} \quad (5)$$

$$V_{out} = A \cdot \overline{B} + \overline{A} \cdot B \quad (6)$$

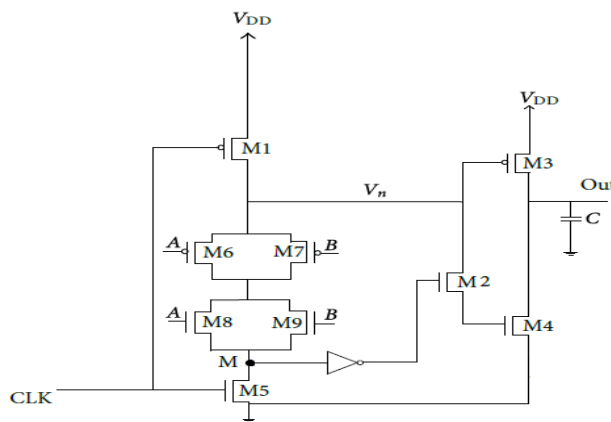


Figure 3: Suggested domino XOR gate.

3.2. Proposed Circuit 2

Here all transistors that can be activated during precharge phase have high threshold voltage transistors and others have low threshold voltage transistors that determine the speed of this circuit. Subthreshold and gate oxide leakage current of all the high- V_t transistors are lesser than low- V_t transistor. In precharge mode, turning on the high- V_t pull-up transistor. When clock is high, operation of this circuit is similar to previous technique.

4. Simulation results

In this section, we compare our proposed circuits with standard N-type Domino XOR gate (DXN), standard P-type domino XOR gate (DXP), Hybrid domino XOR gate with low threshold voltage transistors (DXHL) as shown in Figure 4 and Hybrid domino XOR gate with dual threshold voltage transistors (DXHD).

These circuits have been simulated using 45nm models in Hspice. 1GHz Frequency with 50% Duty Cycle is applied to all circuits. A load capacitance of 0.1pF is also considered. The supply voltage is equal to 0.8 V. The comparison is done in the same condition at room temperature. Figure 5 and Figure 6 shows input and output signals in the suggested circuits.

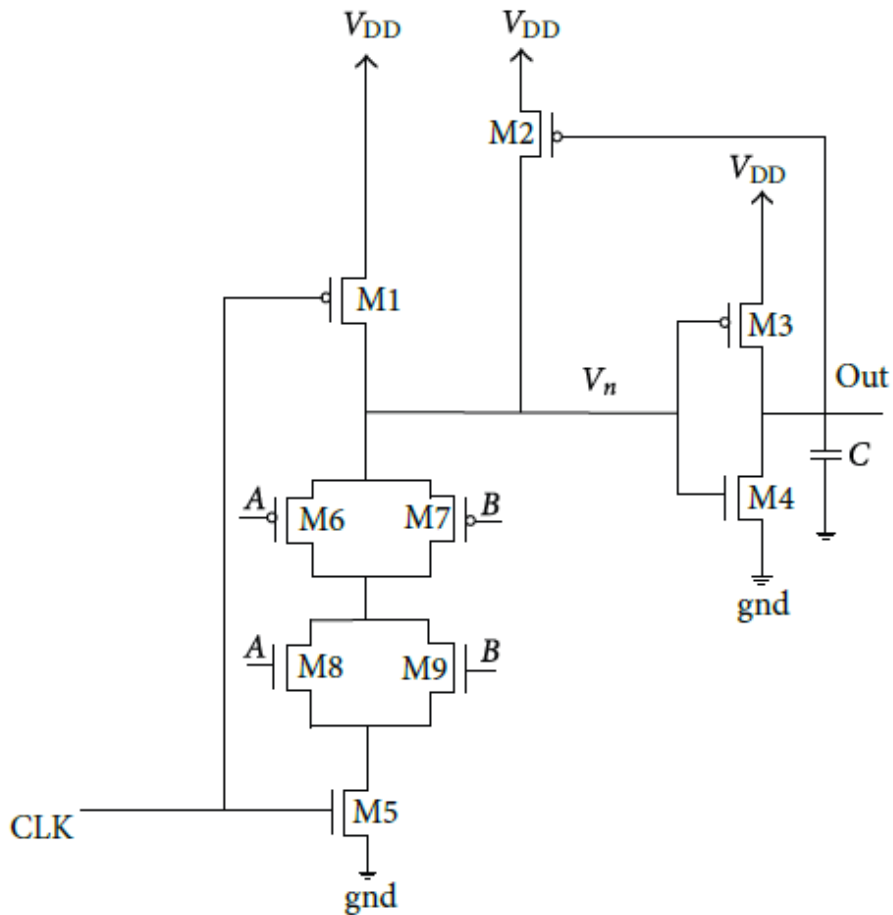


Figure 4: Hybrid domino XOR gate with low threshold. [15]

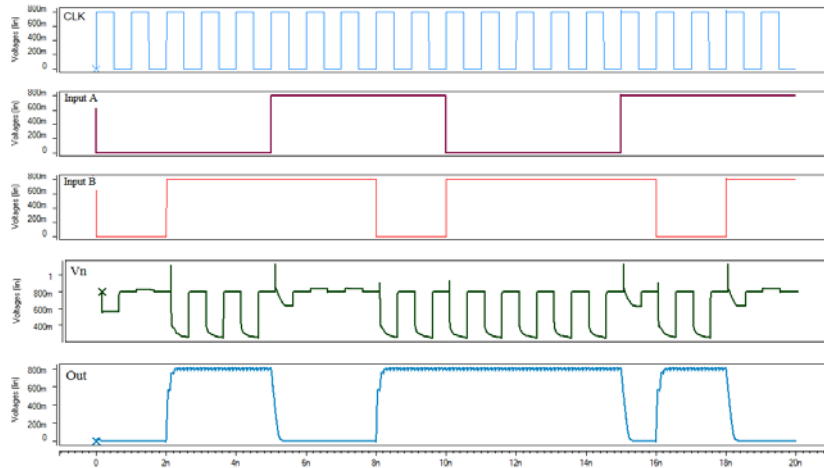


Figure 5: The signal input and output circuit 1

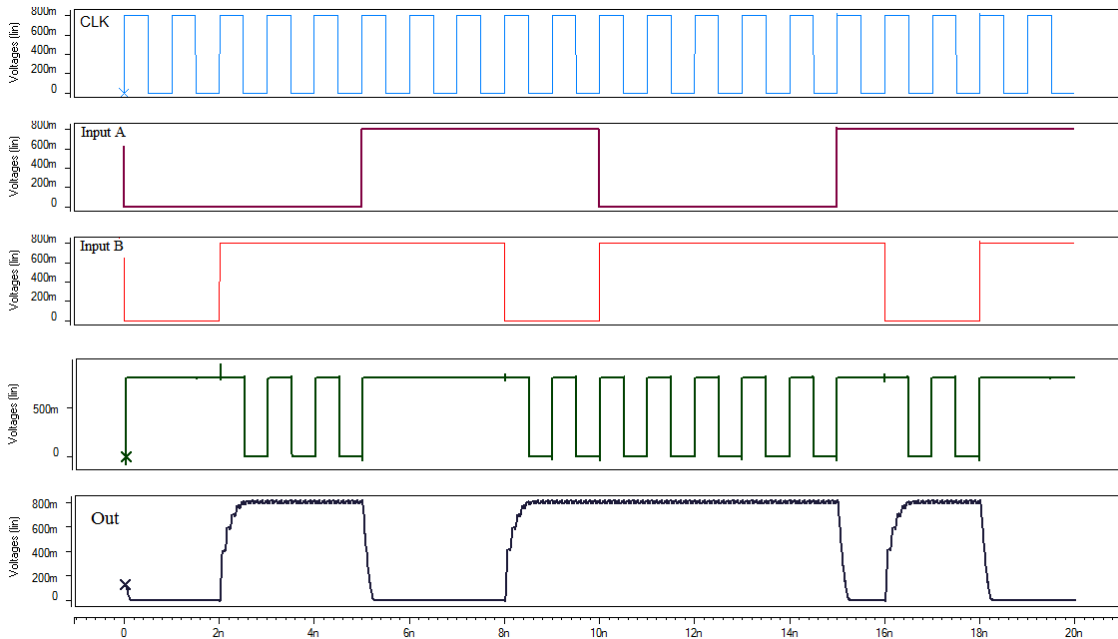


Figure 6: The signal input and output circuit 2

Each of the circuits power consumption with different input combinations is measured in terms of micro-watt as displayed in Table 1.

Furthermore, the reduction in power consumption compared to other circuits is shown in Table 2. According to Table 2, we see that the proposed circuit 2 power consumption compared to standard N-type Domino XOR gate (DXN) is lowered by 81.43%, standard P-type Domino XOR gate (DXP) is lowered by 59.98%, Hybrid domino XOR gate with low threshold voltage transistors (DXHL) is lowered by 41.29%, Hybrid domino XOR gate with dual threshold voltage transistors (DXHD) is lowered by 18.93% and proposed circuit 1 has decreased by 11.94%.

Table 1: Comparison of power consumption in a circuit with different inputs

INPUT	DXN	DXP	DXHL	DXHD	Suggested Circuit1	Suggested Circuit2
A=0 B=0	0.349	0.212	0.271	0.241	0.131	0.114
A=1 B=0	71.05	32.96	22.47	16.27	14.98	13.19
A=0 B=1	71.05	32.96	22.47	16.27	14.98	13.19
A=1 B=1	0.439	0.0322	0.0423	0.0544	0.0298	0.0385

Table 2: Percentage of power reduction compared to other circuits

INPUT	DXN	DXP	DXHL	DXHD	Suggested Circuit1
A=0 B=0	67.33%	46.22%	57.93%	52.69%	12.97%
A=1 B=0	81.43%	59.98%	41.29%	18.93%	11.94%
A=0 B=1	81.43%	59.98%	41.29%	18.93%	11.94%
A=1 B=1	91.23%	-19.56%	8.98%	29.22%	-29.19%

Table 3: Power delay product (pdp) in other circuits

DXN	DXP	DXHL	DXHD	Suggested Circuit 1
602.25	657.59	518.88	210.16	346.12

Table 4: a.c noise margin of four xor circuits

DXN	DXP	DXHL	DXHD	Suggested Circuit 1	Suggested Circuit 2
0.45 V	0.48	0.52	0.56	0.56	0.58

5. Conclusion

In this paper, two new domino XOR circuits are proposed in which by using a combination of N-type and P-type transistors could benefit from high-speed N-type and low power consumption P-type transistors together. In addition to reducing power consumption, we have reduced circuit layout area too. On the other hand we were able to make additional changes in the output node to minimize switching circuit which reduces the power consumption of the circuit.

A proposed circuit adopts hybrid topology with dual threshold voltage transistors. The proposed circuits uses 45nm technology in HSPICE simulation software. Proposed circuit 2 reduces active mode power consumption by 81.43%, 59.98%, 41.29%, 18.93% and 11.94% as compared to standard N-type domino XOR, P-type domino XOR, DXHL, DXHD and proposed circuit 1. Proposed circuit reduces PDP by 69%, 71.61%, 64.02%, 11.18% and 46.07% as compared to standard N-type domino XOR, P-type domino XOR, DXHL, DXHD and proposed circuit 1. Proposed circuit increases A.C noise margin by 28.88%, 17.24%, 10.34%, 5.17% and 3.44% as compared to standard N-type domino XOR, P-type domino XOR, Hybrid domino XOR gate with low threshold voltage transistors, Hybrid domino XOR gate with dual threshold voltage transistors and proposed circuit 1.

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