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Intelligent Clock Gating for FPGA-based RISC Architectures: A Novel Approach to Switching Activity and Dynamic Power Reduction

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Abstract

In modern digital systems, dynamic power consumption remains a critical concern, particularly in Field-Programmable Gate Arrays (FPGAs) utilized in power-sensitive applications. This paper presents a novel intelligent clock gating technique specifically tailored for FPGA-based RISC architectures to effectively reduce switching activity and dynamic power dissipation. Our approach leverages a combination of hardware and software strategies to dynamically control the clock signals to inactive modules, thereby minimizing unnecessary power consumption. The proposed method integrates seamlessly with existing FPGA design flows and RISC architectures, providing a scalable and efficient solution for power management. Through comprehensive simulations and experimental evaluations on standard benchmark circuits, we demonstrate a significant reduction in dynamic power consumption while maintaining performance and functionality. At higher frequencies overall 64% power on total power is saved.

Keywords: Intelligent Clock Gating; FPGA; Switching Activity Reduction; Dynamic Power; RISC.

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1. Introduction

Field Programmable Gate Arrays (FPGAs) are crucial in modern digital system design due to their reconfigurability and high performance, making them suitable for applications ranging from consumer electronics to aerospace. Their flexibility allows post-manufacturing programming, unlike Application-Specific Integrated Circuits (ASICs), which are fixed-function [1].

RISC (Reduced Instruction Set Computing) architectures are often implemented on FPGAs because of their simplicity and efficiency. RISC processors use a small set of simple instructions, enabling faster execution and lower power consumption compared to Complex Instruction Set Computing (CISC) architectures [2].

However, FPGAs and RISC architectures face significant challenges related to high power consumption. In digital circuits, power consumption is categorized into static power (leakage power) and dynamic power. Static power results from leakage currents even when transistors are not switching. Dynamic power, the focus of this study, is consumed during active switching of transistors, involving the charging and discharging of capacitive loads during signal transitions [3].

Dynamic power is primarily influenced by clock signals driving synchronous circuits within an FPGA. Each clock signal transition causes switching activity, leading to dynamic power consumption. This issue is exacerbated in modern high-density FPGAs, where extensive switching activity results in significant power dissipation, thermal challenges, and reduced battery life in portable applications [4].

Traditional power reduction techniques, such as static clock gating, provide a basic method for managing dynamic power. Static clock gating disables the clock signal to parts of the circuit not in use during specific periods. However, these techniques are limited by their inability to adapt to the dynamic nature of real-time workloads, often failing to achieve optimal power savings in scenarios with significant workload variations [5].

This paper addresses the limitations of traditional clock gating by introducing an intelligent clock gating methodology tailored for RISC-based FPGA architectures. The primary objective is to develop a dynamic, adaptive approach that minimizes switching activity and reduces dynamic power consumption without compromising system performance.

The proposed intelligent clock gating technique uses real-time analysis of switching activity to inform clock signal control decisions. By continuously monitoring the activity in different FPGA sections and dynamically adjusting clock gating, substantial reductions in dynamic power consumption can be achieved. This adaptive approach ensures that clock signals are enabled only when necessary, minimizing unnecessary power dissipation.

In summary, our intelligent clock gating method leverages real-time activity monitoring and dynamic control to reduce dynamic power consumption effectively. This novel approach addresses the limitations of static clock gating techniques, offering a significant advancement in managing power consumption in RISC-based FPGA architectures.

2. Background and Related Work

Power consumption in FPGAs has been a significant focus of research due to the increasing demand for energy-efficient designs in both high-performance and embedded systems. FPGAs consume power through both static and dynamic mechanisms. Static power, primarily due to leakage currents, has become more pronounced with the scaling down of transistor sizes [9]. Dynamic power, on the other hand, is associated with the charging and discharging of capacitive loads during transistor switching, with clock signals playing a crucial role in this consumption [6].

Clock gating is a well-established technique for reducing dynamic power consumption. It involves selectively turning off the clock signal to parts of the circuit that are not in use, thereby reducing unnecessary switching activities [5]. Traditional static clock gating methods, applied during the design phase, rely on identifying sections of the circuit that can be periodically disabled based on expected operation patterns [11]. These methods, while effective in reducing power consumption to some extent, do not adapt well to real-time workload variations. To address the limitations of static clock gating, researchers have proposed dynamic clock gating techniques. These methods dynamically control the clock signals based on real-time conditions, providing a more adaptive approach to power management [3]. Dynamic clock gating can significantly reduce power consumption by adapting to the actual activity of the circuit, but it requires complex control mechanisms and real-time monitoring [4].

Intelligent clock gating extends dynamic clock gating by incorporating machine learning and predictive algorithms to make more informed decisions about clock control. This approach leverages historical and real-time data to predict idle periods and adjust clock signals accordingly [8]. Intelligent clock gating techniques have shown promise in various applications, including microprocessors and high-performance computing systems, by achieving substantial power savings with minimal performance impact [10].

RISC architectures, known for their simplified instruction sets and efficient execution, are commonly used in FPGA designs. The simplicity of RISC processors allows for easier implementation of power-saving techniques, such as clock gating [2]. The combination of RISC architectures with intelligent clock gating methods has the potential to further enhance power efficiency in FPGA-based systems [7].

Various power optimization techniques have been proposed for FPGAs, ranging from hardware-level modifications to software-level strategies. At the hardware level, techniques such as voltage scaling, power gating, and clock gating are commonly used to reduce power consumption [9]. At the software level, compiler optimizations and workload management strategies are employed to minimize power usage [12]. Several comparative studies have evaluated the effectiveness of various power management techniques in FPGA designs. These studies typically compare static and dynamic clock gating methods, highlighting the advantages and limitations of each approach [9]. Case studies involving real-world FPGA applications provide valuable insights into the practical implementation and benefits of intelligent clock gating [12].

The literature on FPGA power consumption highlights the importance of dynamic and intelligent clock gating techniques for reducing dynamic power consumption. Traditional static clock gating methods provide a

foundation for power management but are limited by their inability to adapt to real-time workload variations. Dynamic clock gating and intelligent clock gating, which leverage real-time data and predictive algorithms, offer significant improvements in power efficiency. The combination of RISC architectures with intelligent clock gating techniques presents a promising approach to enhancing power efficiency in FPGA-based systems. However, challenges related to implementation complexity and algorithm accuracy remain, necessitating further research and development in this area.

3. Clock Gating Techniques

Clock gating is a powerful technique used to reduce dynamic power consumption in digital circuits by selectively disabling the clock signal to certain parts of a circuit when they are not in use.

Basic Clock Gating: Basic clock gating involves inserting gating logic into the clock path to enable or disable the clock signal based on a control condition. This method uses a simple AND gate to control the clock signal. When the control signal is active, the clock signal passes through; otherwise, the clock is disabled, as shown in Figure 1.

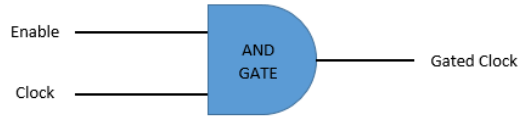

Figure 1: Basic Clock Gating using AND Gate

Integrated clock gating (ICG): An integrated clock gating (ICG) cell, also known as a clock gater cell, controls the clock signal to a group of elements or a sequential element. It's a popular technique in low power design because it saves power by turning off clock signals when registers don't need new input assignments.

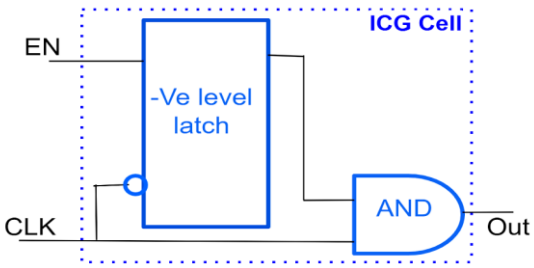

Figure 2: Integrated Clock Gating Cell

Data Driven Clock Gating: Data-driven clock gating in FPGA is a technique aimed at reducing dynamic power consumption by selectively disabling the clock signal to inactive portions of the circuit. The approach involves monitoring data activity and selectively gating clocks, ensuring that only active parts of the circuit consume power. Experimental results demonstrate significant power savings, with minimal impact on overall system latency.

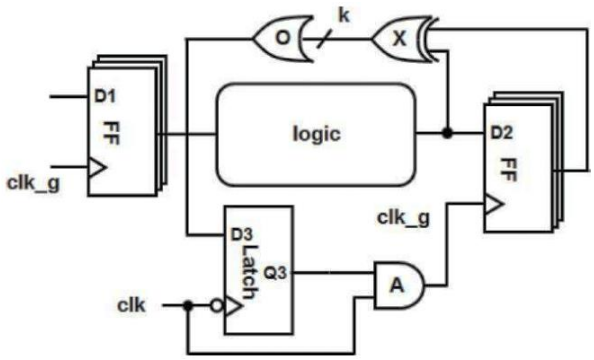

Figure 3: Data Driven Clock Gating

Intelligent clock gating: Intelligent clock gating is a crucial technique for optimizing power consumption in FPGA designs. This method involves selectively disabling the clock signals to certain parts of the design when they are not in use, significantly reducing dynamic power usage. In Vivado, Xilinx's advanced FPGA design suite, intelligent clock gating can be automatically integrated into your design by enabling the power optimization feature, known as **power_opt_design**, during the implementation phase.

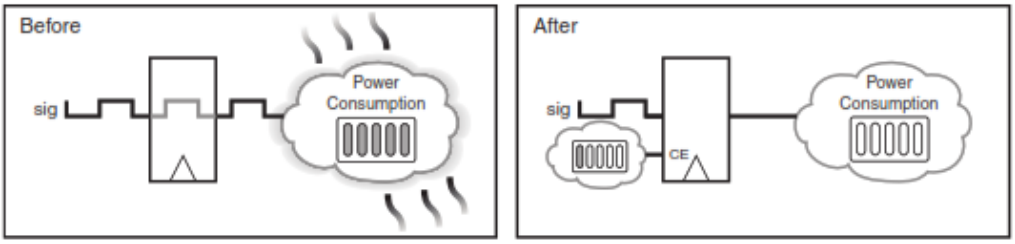

Figure 4: Intelligent Clock Gating Dramatically Reduces Switching Power Consumption

4. Switching Activity estimation in FPGA

Switching activity estimation is critical for low-power FPGA design. Various methods account for circuit delays differently. Zero delay activity assumes no delays, logic delay activity considers only logic delays, and routed delay activity includes both logic and routing delays. Glitches, caused by unequal path delays, increase switching activity, thereby consuming more dynamic power. Glitching can contribute to 20-70% of total power dissipation in ASICs and can be even more significant in FPGAs due to the dominance of interconnect delays. Understanding switching activity under different delay scenarios is crucial for accurate power estimation and low-power synthesis techniques, which often use zero delay data as a baseline [6].In FPGA designs, accurately predicting switching activity and net capacitance is essential for power-aware CAD flows. This paper presents models for early prediction of these parameters, using the Xilinx KC 705 Evaluation Board -28nm Technology Kintex-7 FPGA as a case study. The methodology involves simulation-based approaches to gather switching activity data, considering zero, logic, and routed delays. Using these methods, we assess the impact of glitches and develop prediction models that estimate routed delay activity using zero or logic delay values along with circuit properties. These models are crucial for early power estimation and optimization in FPGA designs.

The Kintex-7 FPGA features array of programmable logic blocks (CLBs) and various interconnect resources. These resources contribute significantly to power consumption, necessitating accurate prediction models for switching activity and capacitance. Our models consider architectural specifics of the FPGA to improve prediction accuracy. For low-power synthesis and early power estimation, accurately predicting switching activity using zero delay data provides a reliable baseline.

5. Experimental Setup and Results

The RISC-32 architecture, known for its simplicity and efficiency in executing instructions, was implemented using pipelining to develop a 32-bit RISC processor. Switching activity was estimated, and clock gating was applied to undesired components and networks. The processor design was captured in Verilog, synthesized using Xilinx Vivado, and then mapped, placed, and routed on an Artix-7 FPGA.

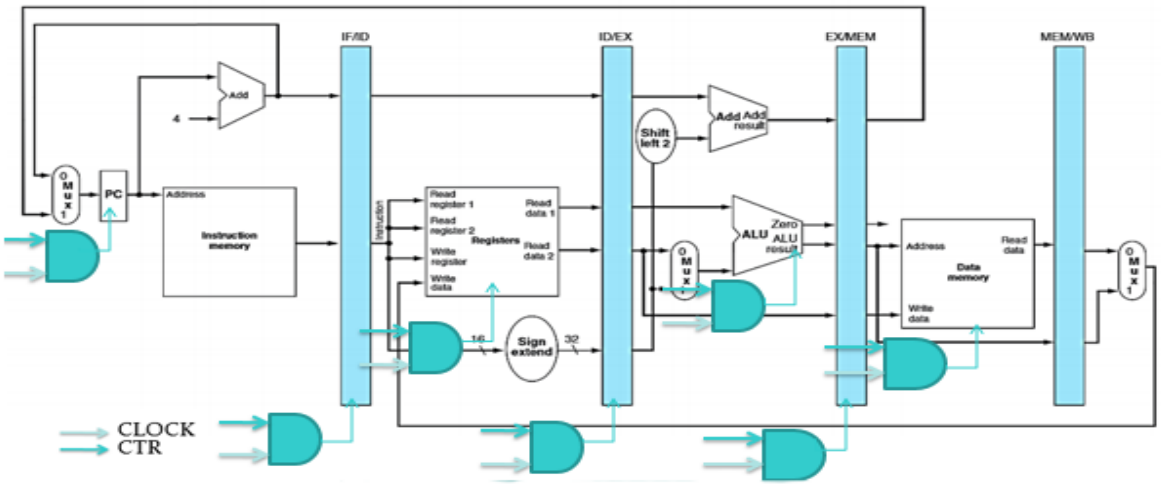

Figure 5: RISC32 Architecture with Clock Gating

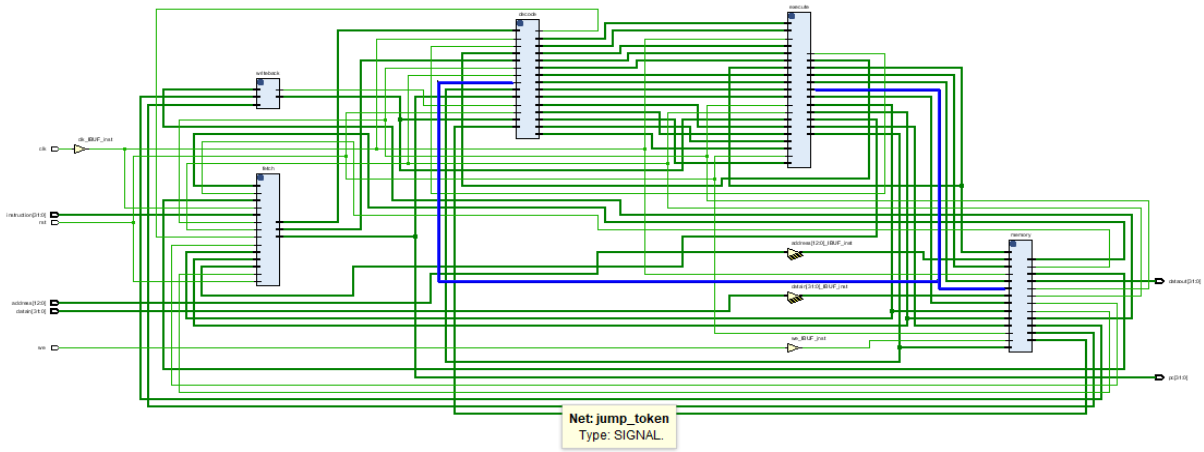

Figure 6: RTL Schematic of RISC 32 Architecture

A comprehensive testbench was developed to simulate real-world operating conditions, covering a wide range of delays, and routed delays to account for different timing scenarios. the processor's functionality. Simulations were performed using Vivado Simulator, considering zero delays, logic Signal transitions for each net were monitored and recorded, and the data was analyzed to extract switching activity information, including the number of transitions per clock cycle and the proportion of time each net spent in high and low states. This activity data was fed into the Xilinx Power Estimator tool to calculate dynamic power consumption, using capacitance and voltage information to provide a detailed power profile.

The RISC processor design included modules such as the instruction fetch unit, decode unit, execution unit, memory access unit, and write-back unit. The instruction fetch unit exhibited high switching activity during the fetch phase, while the execution unit's activity depended on the complexity of the executed instructions. The simulation-based switching activity estimation revealed that the dynamic power consumption of the RISC processor was predominantly influenced by the instruction fetch and execution units, which exhibited the highest switching activity due to their critical roles in the processor's operation.

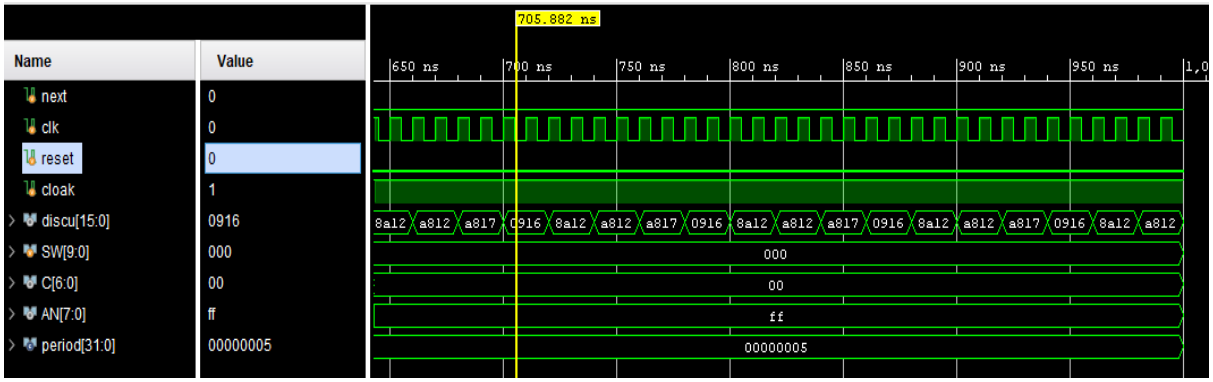

Figure 7: Simulation Waveform of RISC 32 Architecture

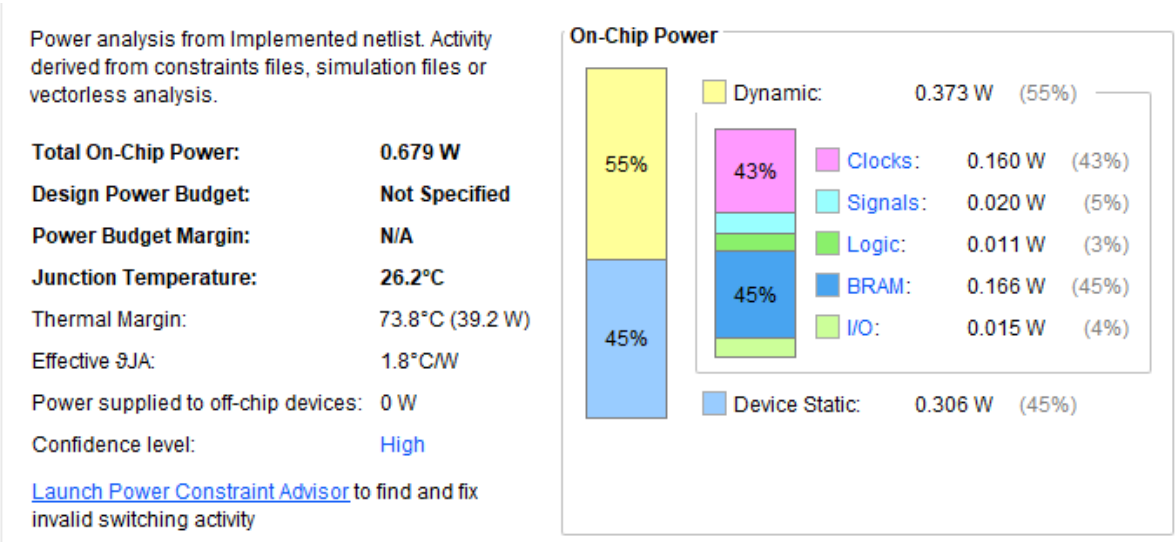

Figure 8: Power Analysis of RISC32 1GHz without clock gating

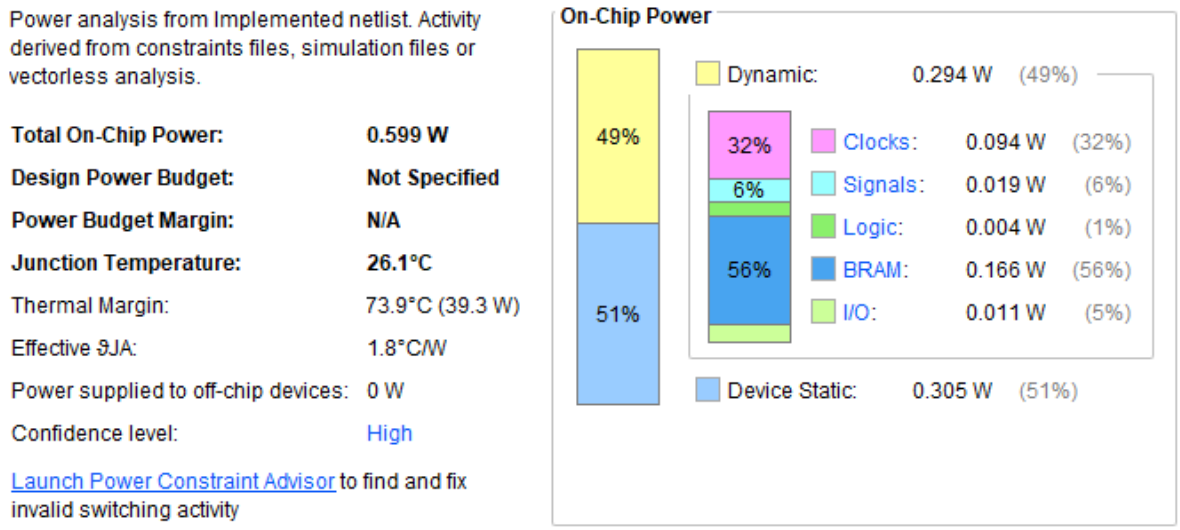

Figure 9: Power Analysis of RISC32 with clock gating

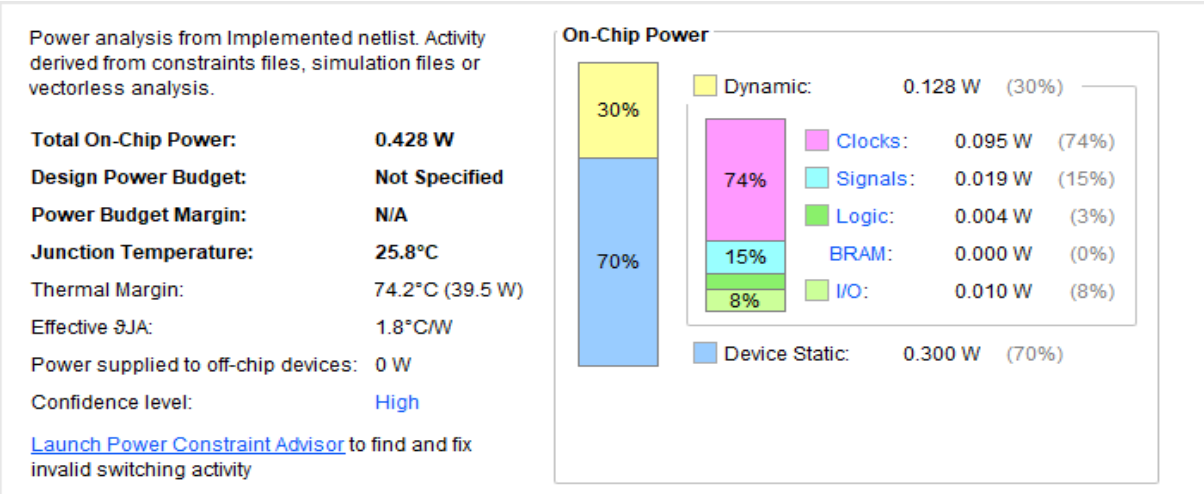

Figure 10: Power Analysis of RISC 32 with Intelligent clock gating and Optimized Switching activity

Table 1: Dynamic power Analysis using clock gating

Frequency	Dynamic Power Consumption			
	Without clock gating	With clock gating	With ICG and Min Switching Activity	% of Total Power saved
100 MHz	69 mw	48 mw	38 mw	44.9%
200 MHz	107 mw	86 mw	62 mw	42%
333 MHz	155 mw	120 mw	86 mw	44.2%
500 MHz	214 mw	164 mw	118 mw	44.8%
1000 MHz	373 mw	294 mw	128 mw	65.6%

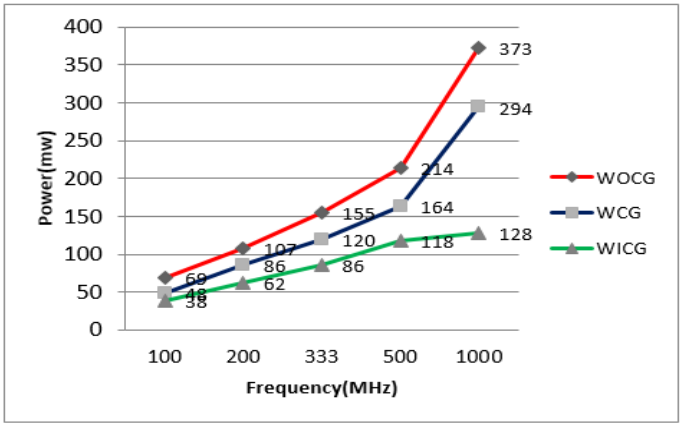

Figure 11: Power Vs Frequency under constant Voltage

Dynamic power consumption was evaluated on different low-power FPGAs using intelligent clock gating techniques to minimize switching activity. The study involved applying these techniques across various FPGA designs and measuring the resulting power savings. Each FPGA's performance was analyzed and compared to determine the effectiveness of intelligent clock gating in reducing dynamic power consumption. The speed-power product is a major concern in low-power designs. Increasing the device speed necessitates an increase in frequency, which in turn results in higher dynamic power consumption. As illustrated in Figure 11, we applied our low-power method to designs operating at different frequencies. The results show a notable decrease in dynamic power consumption by 36%. Moreover, at higher frequencies, the reduction in power consumption exceeded 60% due to the implementation of intelligent clock gating combined with switching activity prediction. Nowadays, various FPGA vendors are providing built-in power reduction methods in their FPGA offerings. We have tested different FPGAs using our design and have also implemented clock gating to further reduce dynamic power consumption.The results, presented in Table 2, provided a comparative and competitive analysis, highlighting the differences in power efficiency among the tested FPGAs. This comprehensive evaluation demonstrated the potential of intelligent clock gating to significantly reduce power consumption in FPGA-based systems.

Table 2: Dynamic power Analysis on Low power FPGAs

FPGA	Dynamic Power Consumption	
	Without CLK-GAT	With ICG and Min Switching activity
Artix-7(AC 701)	302 mw	136 mw
Kintex-7(KC 705)	373 mw	128 mw
Kintex-7(KCU 105)	327 mw	93 mw
Virtex -7 (VCU 118)	354 mw	113 mw
Zynq -706	294 mw	147 mw
Zynq (Ultra Scale)	248 mw	87 w

6. Conclusion

Clock gating has proven to be a highly effective technique for reducing dynamic power consumption in FPGA designs. In this study, we demonstrated a significant overall power savings of 64% at higher frequencies through the application of clock gating across various stages of a RISC-32 processor implemented on an Artix-7 FPGA. By adding latches to inputs with zero switching activity, we achieved an additional 8% reduction in total power consumption. Furthermore, optimizing the switching activity of minimized functional blocks resulted in a reduced toggling rate, enhancing the impact of clock gating. These results highlight the potential of intelligent clock gating and switching activity prediction in achieving substantial power efficiency in FPGA-based systems. The techniques and methodologies developed in this research can be applied to other processor architectures and FPGA designs, paving the way for more energy-efficient and sustainable computing solutions.

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